REMARKS/ARGUMENTS

Claims 1-20 remain in the application. Claims 1, 2, 8, 11-14, 16, 19 and 20 are amended.

Claim Objections

Claims 1-20 were objected to for various informalities which are corrected herein.

Claim Rejections Under 35 USC § 103

Claims 1-20 were rejected under 35 USC § 103(a) over US Patent 5,996,411 to Leonardson, et al. or US Patent 5,948,981 to Woodruff or US Patent 6,269,698 to Woodruff or US Patent 6,453,744 to Williams or US Patent 6,484,578 to Woodruff, et al. in view of US Patent 6,541,369 to Huang, et al.

The invention as originally presented is patentable over all of Leonardson, Woodruff '981, Woodruff '698, Williams, Woodruff '578 and Huang, individually and in combination.

The Examiner contends that the references disclose a vibrating beam accelerometer comprising a beam formed of a semiconductor material; an electrode formed of the semiconductor material spaced from the beam; an insulator layer formed on a surface of the beam and the electrode.

The Examiner contends that the only difference between the prior art and the claimed invention is an electrical charge buried in the insulator layer. The Examiner further contends that Huang, et al. discloses a device for reducing fixed charges in a semiconductor device comprising insulating layers 104,108 having electrical charge 202 buried in the insulator layer. Column 1, line 43 to column 2, line 41. The Examiner further contends that it would have been obvious to a person of ordinary skill in the art at the time of invention to have readily recognized the advantages and desirability of employing an electrical charge buried in the insulator layer as suggested by Huang, et al. to the device of the references to provide a low "k" dielectric material to increase insulative properties, yet not creating the charge trap phenomenon at an interface between such low "k" dielectric material and other insulative materials. See, column 2, lines 42-47 of Huang et al.

The Examiner is mistaken. Huang completely fails to disclose or suggest any desirability of employing an electrical charge buried in the insulator layer. Rather, Huang clearly

states that it is a disadvantage to have such an electrical charge buried in the insulator layer. In the "Description of the Background Art" section, Huang states:

> Integrated circuits fabricated on semiconductor substrates for Ultra Large Scale Integration (ULSI) require multiple levels of interconnections for electrically connecting the discrete semiconductor devices that comprise the circuits. Conventionally, the multiple levels of interconnections are separated by layers of insulating material. These interposed insulating layers have etched via holes which are used to connect one level of interconnections to another. Typically, the insulating layer material is silicon oxide (SiO_2) having a dielectric constant (relative to vacuum) of about 4.1 to 4.5. As device dimensions decrease and the device density increases, it is necessary to reduce the spacing between the interconnection levels to effectively connect the integrated circuits. Unfortunately, as the spacing decreases, the intra-(on the same metal level) and interlevel (between metal levels) capacitances increase when insulating layers therebetween have the same dielectric constant. The capacitance C is inversely proportional to the spacing d between the levels by the relationship C=keA/d where k is the dielectric coefficient, e is the permittivity of the insulator, A is the area, and d is the spacing between lines. Therefore, it is very desirable to minimize the dielectric constant k in the insulating layers between the interconnection layers to reduce the RC time constant and thereby increase the performance of the circuit (frequency response). The signal propagation time in the circuit is adversely affected by the RC delay time, where R is the resistance of the metal line, and C is the inter- and/or the intralevel capacitance mentioned above.
> Column 1, lines 15-42.

Huang reiterates the desirability to minimize the dielectric constant k in the insulating layers, by stating that:

> Therefore, there is a need in the art for a method of semiconductor IC construction and resultant apparatus having low k dielectric material to increase insulative properties, yet not creating the charge trap phenomenon at an interface between

such low k dielectric material and other insulative materials used to construct such a device.

Column 2, lines 42-47.

Thus, Huang clearly states the **undesirability** of employing an electrical charge buried in the insulator layer, as recited in claim 1 of the present invention.

Because Huang clearly teaches only that employing an electrical charge buried in the insulator layer is **undesirable**, Huang clearly fails to provide the deficiencies of the US Patent 5,996,411 to Leonardson, et al., US Patent 5,948,981 to Woodruff, US Patent 6,269,698 to Woodruff, US Patent 6,453,744 to Williams, and US Patent 6,484,578 to Woodruff, as to employing an electrical charge buried in the insulator layer, as originally recited in claim 1. Rather, by teaching only a method and apparatus for reducing trapped charges in a semiconductor device, Huang actually teaches away from having an electrical charge buried in the insulator layer, as recited in claim 1.

For at least the above reasons, claim 1 as originally filed is believed to be allowable.

Therefore, the Applicants respectfully decline to amend claim 1 at this time, except for correcting the informalities.

Claims 2-7 are allowable as depending from allowable claim 1.

Claim 4 is additionally allowable independently of allowable claim 1 as reciting the insulator layer having an electrical charge buried therein further comprising an insulator layer formed on a surface of the electrode facing toward the beam. Huang completely fails to disclose or suggest an electrical charge buried in an insulator layer formed on a surface of the electrode facing toward the beam, as originally recited in claim 4. For at least the above reasons, claim 4 is believed to be allowable independently of allowable claim 1.

Independent claims 8 and 13 differ in scope from allowable claim 1. However, the above arguments directed to claim 1 are sufficiently applicable to claims 8 and 13 as to make repetition unnecessary. Thus, for each of the reasons above, claims 8 and 13 are believed to be allowable over the cited art.

Therefore, the Applicants respectfully decline to amend claims 8 and 13 at this time, except for correcting the informalities.

Claims 9-12 and 14-20 are allowable at least as depending from respective allowable claims 8 and 13.

The claims now being in form for allowance, reconsideration and allowance is respectfully requested.

If the Examiner has questions or wishes to discuss any aspect of the case, the Examiner is encouraged to contact the undersigned at the telephone number given below.

Respectfully submitted,

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